Amendments to the Claims:

Please cancel claims 4-5 as being directed to a non-elected invention. Please amend claim 1 as follows. Please add new claims 6-8 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A duty cycle correction circuit of a delay locked loop, comprising:

a differential amplifier, which receives and amplifies differential reference clock signals through a first input terminal and a second input terminal, and outputs differential output signals to a first differential output terminal and a second differential output terminal, respectively;

a first transmission circuit, which is connected between the first differential output terminal and a first node, and transmits a signal of the first differential output terminal to the first node, in response to transmission control signals;

a second transmission circuit, which is connected between the second differential output terminal and a second node, and transmits a signal of the second differential output terminal to the second node, in response to the transmission control signals;

a first storage unit, which is connected between the first node and a ground voltage and accumulates electric charges on the first node;

a second storage unit, which is connected between the second node and the ground voltage and accumulates electric charges on the second node; and

a current control circuit, which controls an amount of electric charges accumulated in the first storage unit and an amount of electric charges accumulated in the second storage unit, in response to a combination of duty cycle switching signals and corresponding current switching control ~~signal~~ signals.

2. (Original) The duty cycle correction circuit of claim 1, wherein each of the first

transmission circuit and the second transmission circuit is a transmission gate.

3. (Original) The duty cycle correction circuit of claim 1, wherein each of the first storage unit and the second storage unit is a MOS transistor.

4.- 5. (Canceled)

6. (New) The duty cycle correction circuit of claim 1, wherein the duty cycle switching signals comprise a duty cycle reduction signal and a duty cycle enhancement signal.

7. (New) The duty cycle correction circuit of claim 6, wherein one of the duty cycle reduction signal and the duty cycle enhancement signal is activated at one time.

8. (New) The duty cycle correction circuit of claim 6, wherein a combination of the duty cycle reduction signal and at least one active corresponding switching control signal reduces the amount of electric charges accumulated in the first storage unit.